

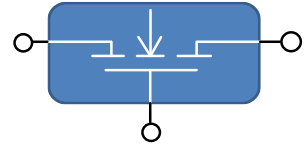
# INN040W080A

## 1. General Description

Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 1.7 mm x 1.7 mm package size.

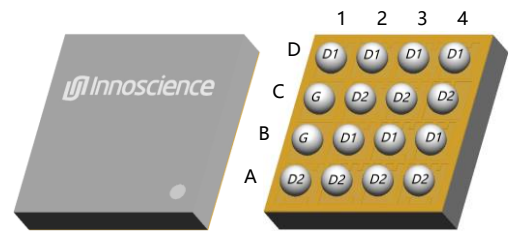
## 2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance



## 3. Applications

- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power suppliers system



## 4. Key Performance Parameters

**Table 1** Key performance parameters at  $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DD,max}$	40	V
$R_{D1D2(on),max}$ @ $V_G = 5\text{ V}$	8	m $\Omega$
$Q_{G,typ}$ @ $V_{DD} = 20\text{ V}$	10.1	nC
$I_{D,DC}$	14	A

## 5. Pin Information

**Table 2** Pin information

Pin	Pin description	Pin function
D1~4, B2~4	Drain1	Power Drain1
C2~4, A1~4	Drain2	Power Drain2
B1, C1	Gate	Driver Gate

**Table 3** Ordering information

Type/Ordering Code	Package	Product Code
INN040W080A	WLCSP 1.7x1.7	D16

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## 6. Maximum Ratings

at  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

**Table 4** Maximum ratings

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MAX</b>	<b>UNIT</b>
$V_{DD}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	40	V
$V_{DG}$	Drain-to-Gate Voltage	40	V
$V_{GD}$	Gate-to-Drain Voltage	6	V
$I_D$	Continuous Drain current (limited by solder ball)	14	A
$I_{DM}$	Pulsed Drain Current ( $25^\circ\text{C}$ , $T_{Pulse} = 300\text{ }\mu\text{s}$ )	70	A
$P_{tot}$	Power dissipation ( $T_{c, bottom} = 25^\circ\text{C}$ )	15	W
$T_J$	Operating Temperature	-40 to 125	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	$^\circ\text{C}$

## 7. Thermal Characteristics

**Table 5 Thermal characteristics**

SYMBOL	PARAMETER	TYP	UNIT
R <sub>θJC_top</sub>	Thermal Resistance, Junction to Case (top)	0.97	°C/W
R <sub>θJC_bot</sub>	Thermal Resistance, Junction to Case (bottom)	6.61	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient <sup>1</sup>	65.12	°C/W

Note 1: R<sub>θJA</sub> is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

## 8. Electric Characteristics

 at  $T_J = 25\text{ }^\circ\text{C}$ , unless specified otherwise

**Table 6** Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$BV_{D1D2S}$	Drain1-to-Drain2 Breakdown Voltage	40			V	$V_{D2} = V_G = 0\text{ V}$ , $I_{D1D2} = 500\text{ }\mu\text{A}$
$BV_{D2D1S}$	Drain2-to-Drain1 Breakdown Voltage	40			V	$V_{D1} = V_G = 0\text{ V}$ , $I_{D2D1} = 500\text{ }\mu\text{A}$
$I_{D1D2S}$	Zero Gate Voltage Drain Current			20	$\mu\text{A}$	$V_{D2} = V_G = 0\text{ V}$ , $V_{D1} = 40\text{ V}$
$I_{D2D1S}$	Zero Gate Voltage Drain Current			20	$\mu\text{A}$	$V_{D1} = V_G = 0\text{ V}$ , $V_{D2} = 40\text{ V}$
$I_{GDS}$ ( $T_J = 85\text{ }^\circ\text{C}$ )	Gate-to-Drain Leakage		0.5	5	$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = 5\text{ V}$
	Gate-to-Drain Leakage	-30			$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = -5\text{ V}$
$I_{GDS}$ ( $T_J = 85\text{ }^\circ\text{C}$ )	Gate-to-Drain Leakage		5	30	$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = 6\text{ V}$
	Gate-to-Drain Leakage	-40			$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = -6\text{ V}$
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D1} = 0\text{ V}$ , $V_{D2} = V_G$ , $I_{D2D1} = 1\text{ mA}$
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D2} = 0\text{ V}$ , $V_{D1} = V_G$ , $I_{D1D2} = 1\text{ mA}$
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance		6.1	8	m $\Omega$	$V_{D2} = 0\text{ V}$ , $V_{GD} = 5\text{ V}$ , $I_{D1D2} = 10\text{ A}$
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance		6.1	8	m $\Omega$	$V_{D1} = 0\text{ V}$ , $V_{GD} = 5\text{ V}$ , $I_{D2D1} = 10\text{ A}$

**Table 7 Dynamic characteristics**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C <sub>ISS</sub>	Input Capacitance		566		pF	V <sub>G</sub> = 0 V, V <sub>D</sub> = 20 V
C <sub>OSS</sub>	Output Capacitance		243			
C <sub>RSS</sub>	Reverse Transfer Capacitance		145			
R <sub>G</sub>	Gate Resistance		4.1		Ω	f = 1 MHz
Q <sub>G</sub>	Total Gate Charge		10.1		nC	V <sub>D</sub> = 20 V, V <sub>G</sub> = 5 V, I <sub>D</sub> = 10 A
Q <sub>GD1</sub>	Gate-to-Drain1 Charge (V <sub>D2D1</sub> =20V)		1.2			V <sub>D1</sub> = 0, V <sub>D2</sub> = 20 V, I <sub>D2D1</sub> = 10 A
Q <sub>GD1</sub>	Gate-to-Drain1 Charge (V <sub>D1D2</sub> =20V)		5.5			V <sub>D2</sub> = 0, V <sub>D1</sub> = 20 V, I <sub>D1D2</sub> = 10 A
Q <sub>GD2</sub>	Gate-to-Drain2 Charge (V <sub>D1D2</sub> =20V)		1.2			V <sub>D2</sub> = 0, V <sub>D1</sub> = 20 V, I <sub>D1D2</sub> = 10 A
Q <sub>GD2</sub>	Gate-to-Drain2 Charge (V <sub>D2D1</sub> =20V)		5.5			V <sub>D1</sub> = 0, V <sub>D2</sub> = 20 V, I <sub>D2D1</sub> = 10 A
Q <sub>OSS</sub>	Output Charge		8			V <sub>G</sub> = 0 V, V <sub>D</sub> = 20 V

## 9. Electric Characteristics Diagrams

at  $T_J = 25\text{ }^\circ\text{C}$ , unless specified otherwise

Note: In Charts, VD1D2 can be VD2D1 with same characteristic chart due to Bi-directional feature.

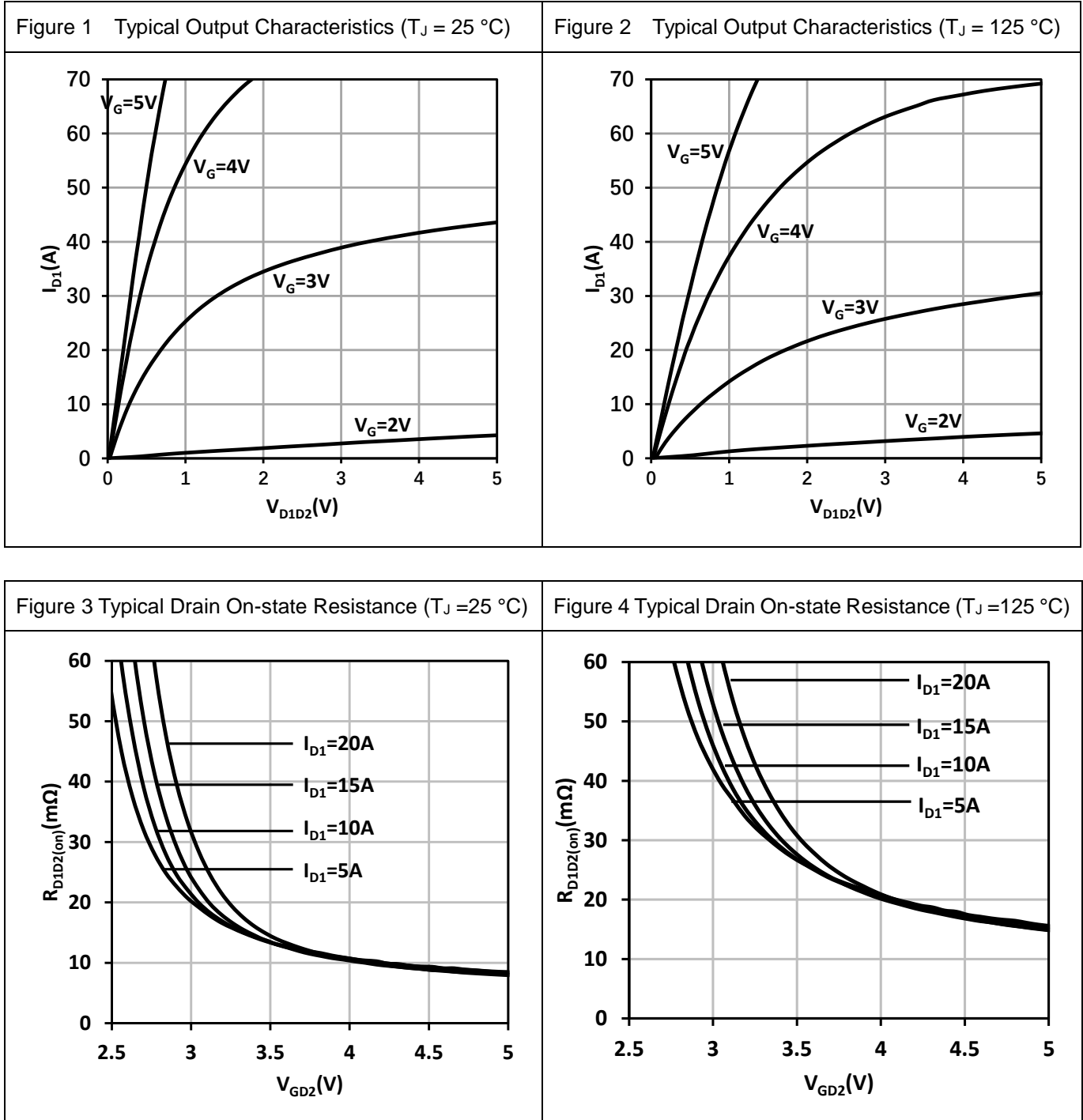


Figure 5 Typical On Resistance vs. Temperature

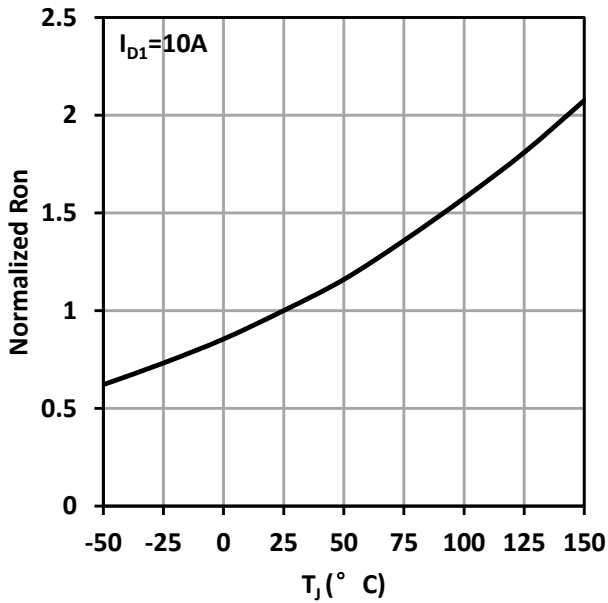


Figure 6 Typical Transfer Characteristics

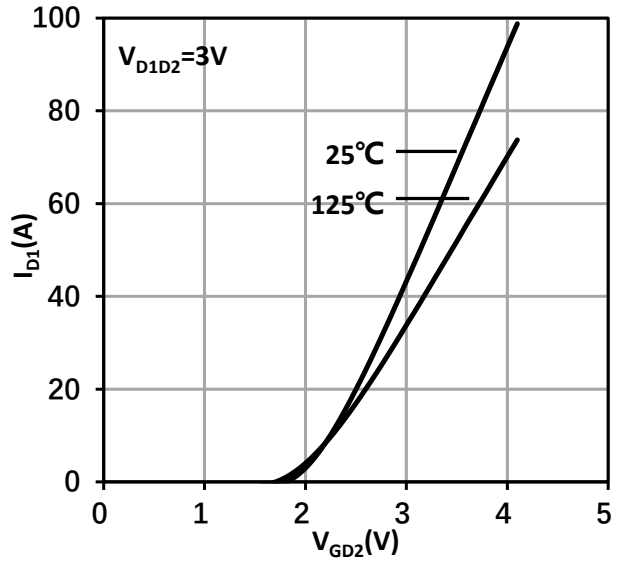


Figure 7 Typ. Reverse Drain1- Drain2 Characteristics ( $V_{GD2} \leq 0V$ ,  $T_J = 25^\circ C$ )

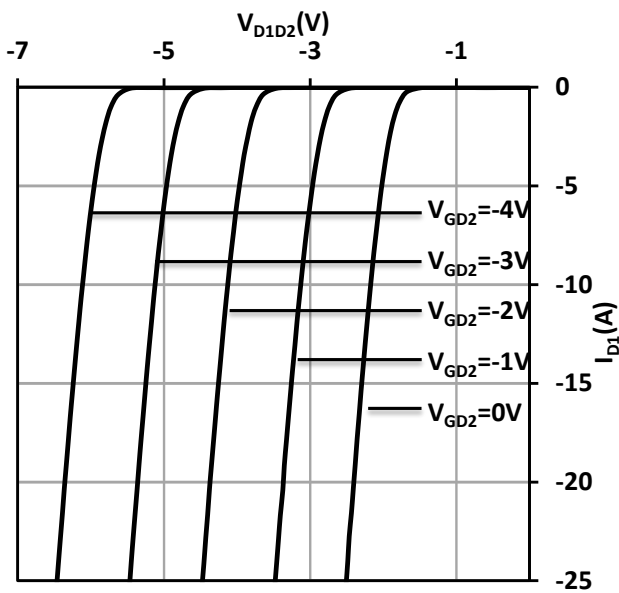


Figure 8 Typ. Reverse Drain1- Drain2 Characteristics ( $V_{GD2} \geq 0V$ ,  $T_J = 25^\circ C$ )

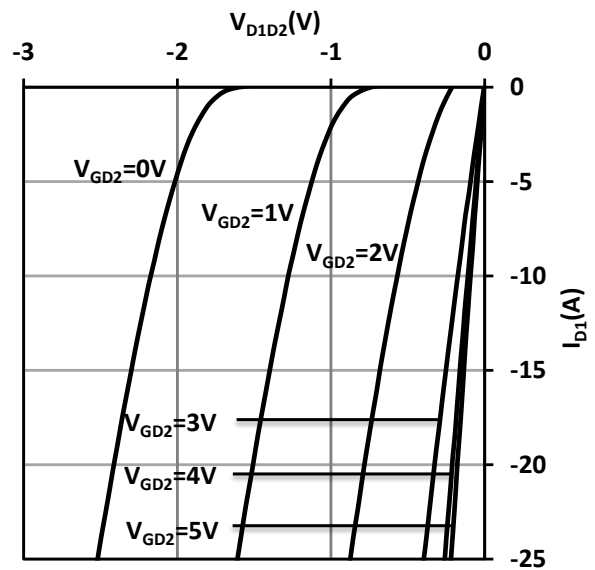




Figure 9 Typ. Reverse Drain1- Drain2 Characteristics ( $V_{GD2} \leq 0V$ ,  $T_J = 125\text{ }^\circ\text{C}$ )

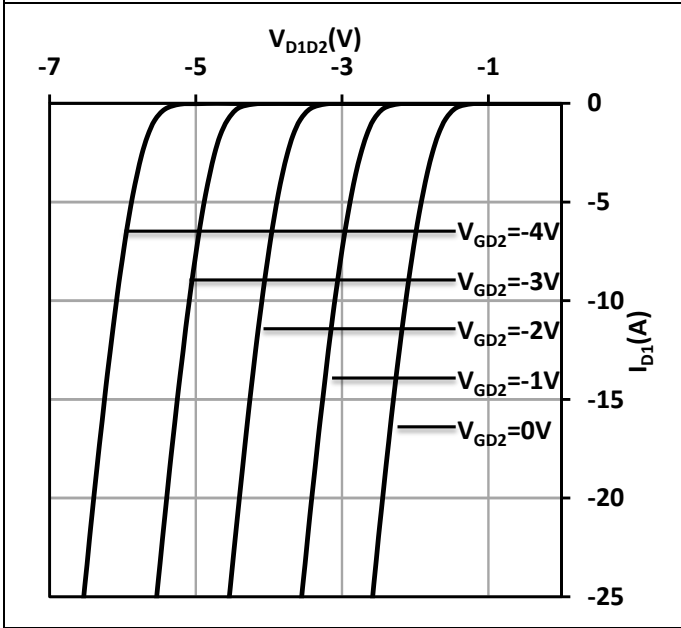


Figure 10 Typ. Reverse Drain1-Drain2 Characteristics ( $V_{GD2} \geq 0V$ ,  $T_J = 125\text{ }^\circ\text{C}$ )

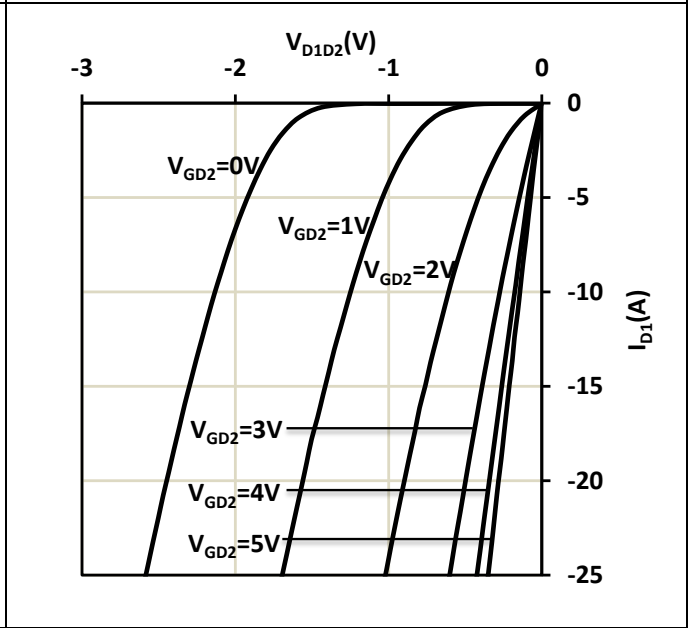


Figure 11 Typ. Capacitances Characteristics

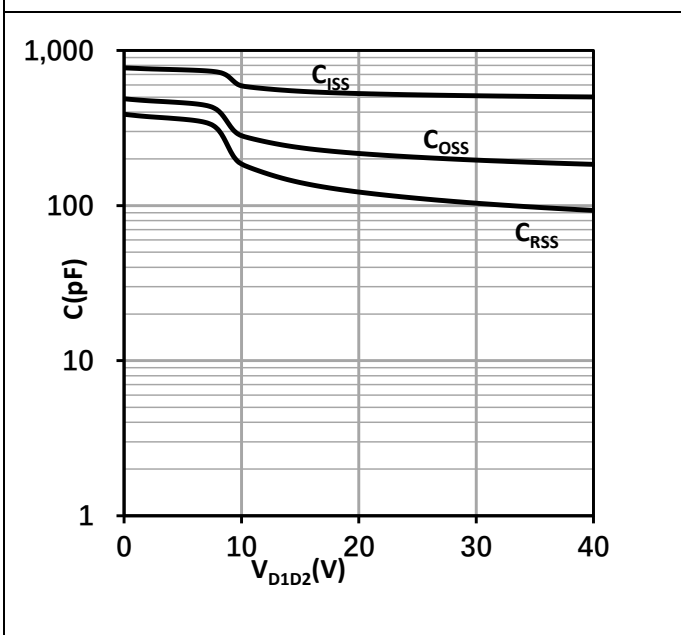


Figure 12 Typ. Gate Charge

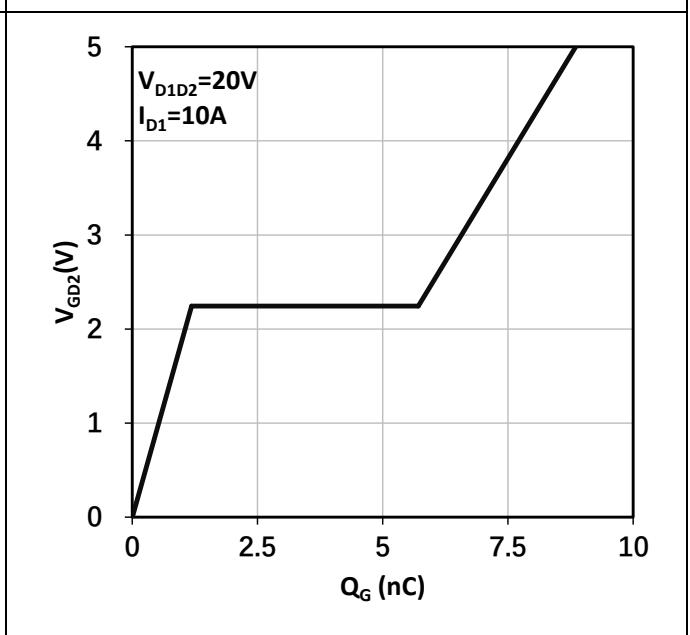


Figure 13 Normalized Threshold Voltage vs. Temp.

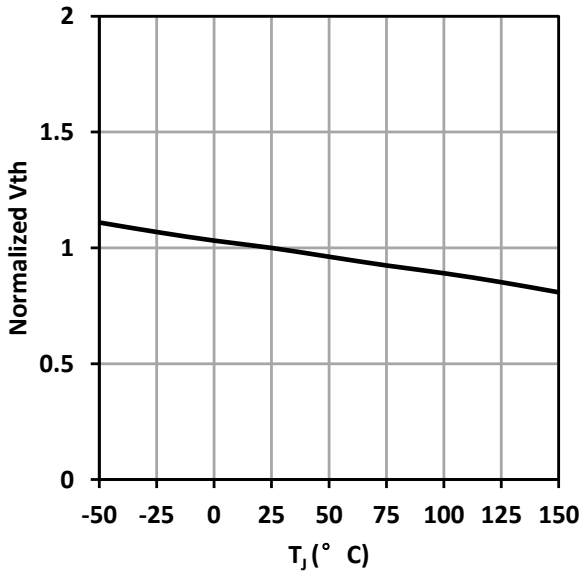


Figure 14 Output Charge

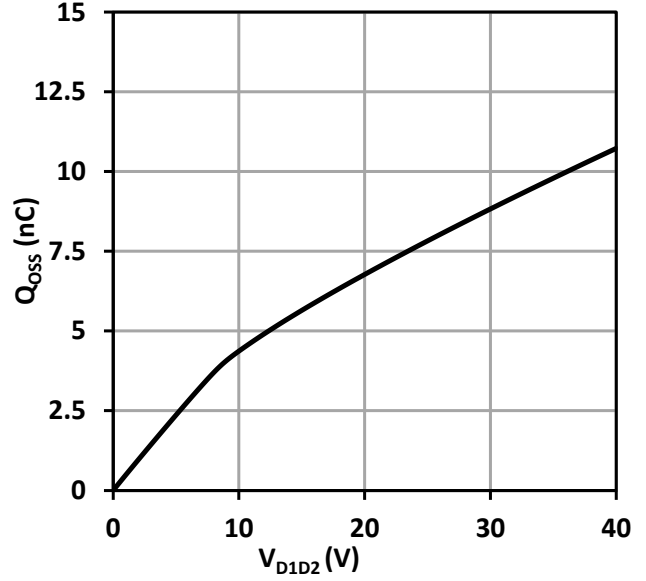


Figure 15 Output Capacitance Stored Energy

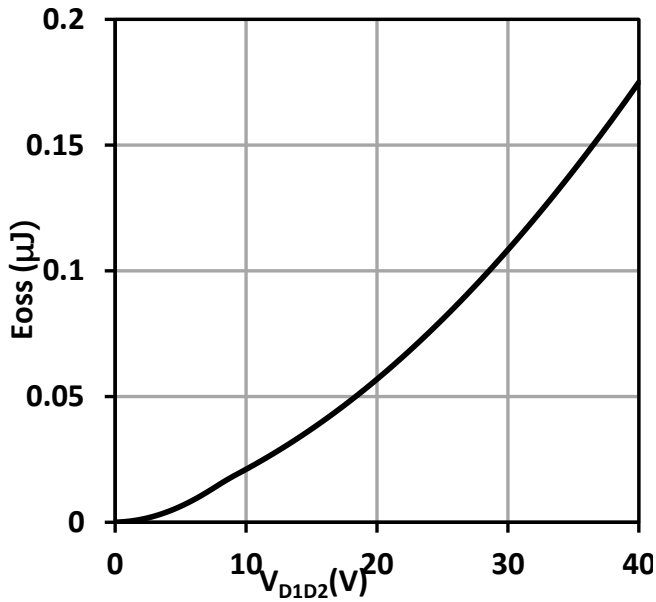


Figure 16 Power Dissipation

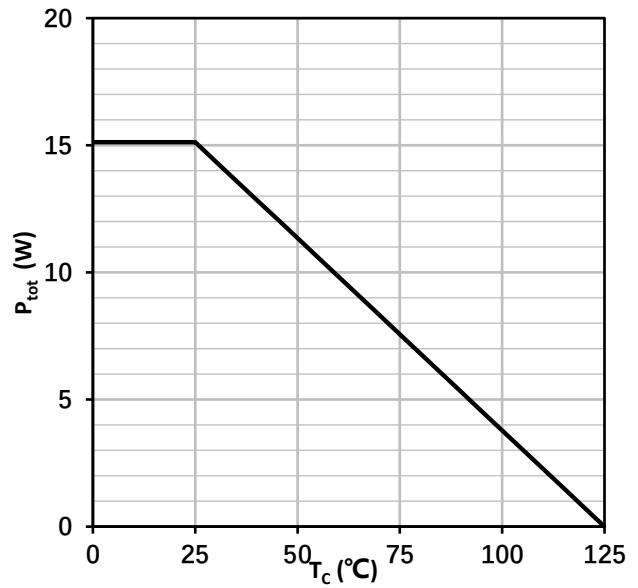


Figure 17 Safe Operating Area

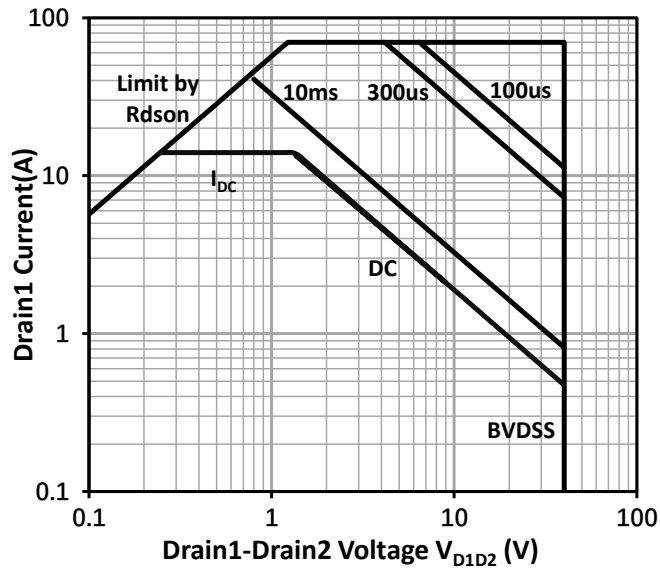
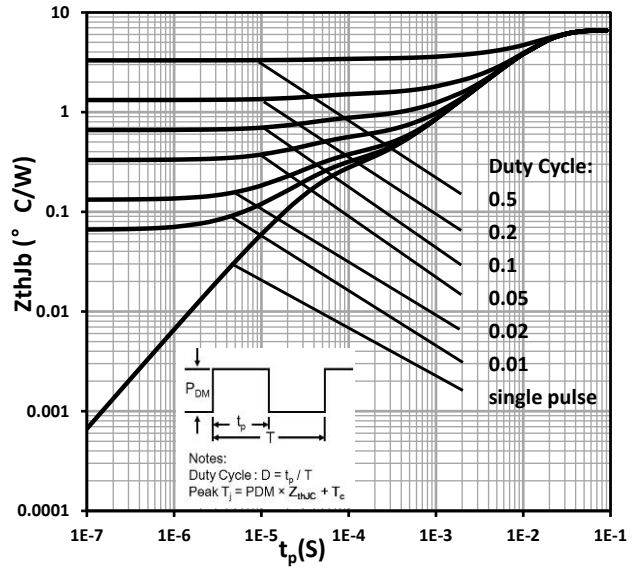
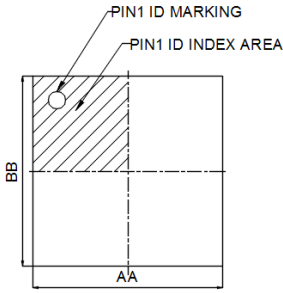


Figure 18 Max. Transient Thermal Impedance

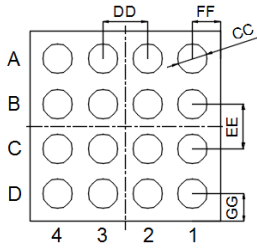


## 10. Package Outlines

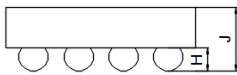
### Package Reference



TOP VIEW



BOTTOM VIEW



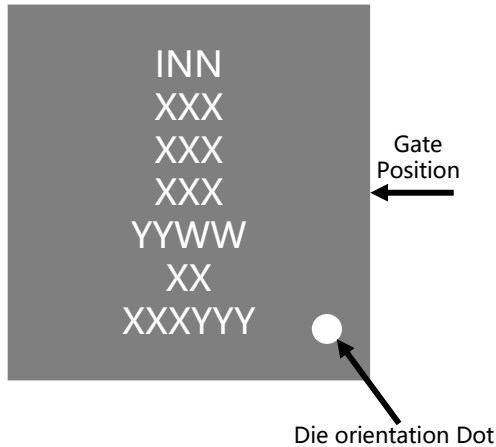
SIDE VIEW

SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
AA	1.675	1.700	1.725	
BB	1.675	1.700	1.725	
CC	0.241	0.268	0.295	16X
DD	0.400 BASIC			12X
EE	0.400 BASIC			12X
FF	0.250 REF			4X
GG	0.250 REF			4X
H	0.175	0.205	0.235	
J	0.517	0.564	0.611	

**NOTE:**

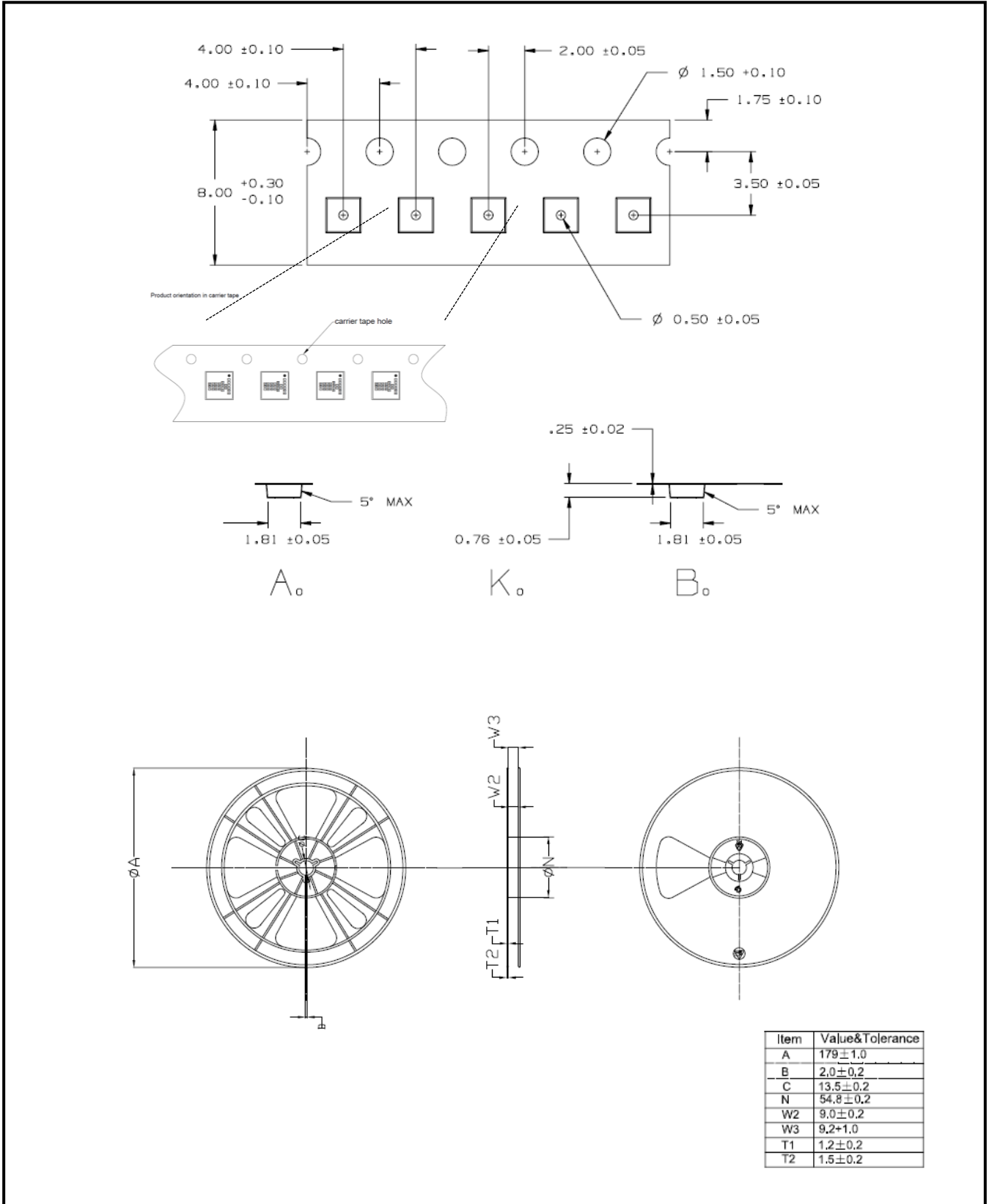
- 1) ALL DIMENSION ARE IN MILLIMETERS.
- 2) BOTTOM VIEW IS SOLDER BALL VIEW.
- 3) COMPLIES WITH JEDEC MO-211.
- 4) DRAWING IS NOT TO SCALE.
- 5) A,B IS PACKAGE SIZE
- 6) BAR COPLANARITY SHALL BE 0.05 MILLIMETERS MAX

### Marking Reference:



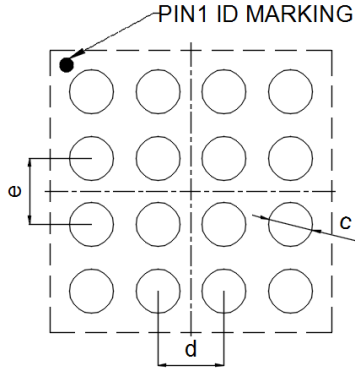
Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Lot code	XXX
Row 4		XXX
Row 5	Date code	YYWW
Row 6	Wafer ID	XX
Row 7	Location ID	XXXYYY

### 11. Reel Information



**12. Land Pattern**

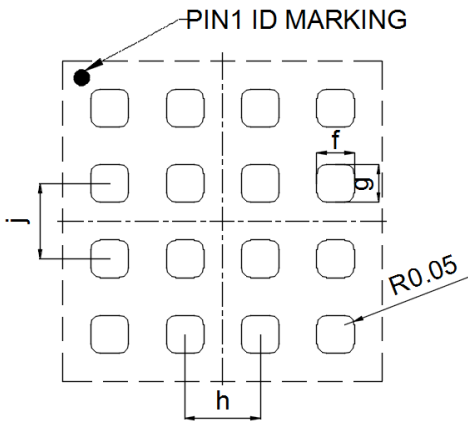
**Recommended Land Pattern**



TOP VIEW

SYMBOL	MILLIMETER	NOTE
	NOM	
c	0.214	16X
d	0.400 BASIC	12X
e	0.400 BASIC	12X

**Recommended Stencil Drawing**



TOP VIEW

SYMBOL	MILLIMETER	NOTE
	NOM	
f	0.200	16X
g	0.200	16X
h	0.400 BASIC	12X
j	0.400 BASIC	12X

## 13. Revision History

### Major changes since the last revision

Revision	Date	Description of changes
1.0	2023-01-10	1.0 version release
1.1	2023-08-14	<ol style="list-style-type: none"><li>1. Updated format and corrected typos</li><li>2. Added <math>P_{tot}</math> in Maximum Ratings</li><li>3. Corrected description 'D' to 'D1', 'S' to 'D2' in Electric Characteristics Diagrams</li><li>4. Updated Note in Electric Characteristics Diagrams</li></ol>

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## Important Notice

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